CLAIMS

What is claimed is:

1. A method for testing a plurality of semiconductor components, comprising:

forming a plurality of dice on a semiconductor wafer, said plurality of dice each including at least one die contact; and

forming at least one wafer-level redistribution circuit on each of said plurality of dice for interconnection with others of said plurality of dice, said at least one wafer-level redistribution circuit including a redistribution circuit a bus conductor traversing each of said plurality of dice for electrically coupling with at least another one of said plurality of dice and at least one conductor for coupling said redistribution circuit to said bus conductor.

2. The method, as recited in claim 1, further comprising forming an outer passivation layer on an exposed face of said semiconductor wafer covering said redistribution circuit and said bus conductor.

3. The method, as recited in claim 2, further comprising probing each of said plurality of dice to determine functional and nonfunctional dice.

4. The method, as recited in claim 3, further comprising storing location information on nonfunctional dice.

5. The method, as recited in claim 4, further comprising isolating at least one die contact on each of said nonfunctional dice.

6. The method, as recited in claim 5, wherein said isolating includes removing a portion of said outer passivation layer over said at least one of said redistribution circuit and said bus connector to form an open circuit between said at least one die contact and said bus conductor on said nonfunctional dice.

7. The method, as recited in claim 5, wherein said isolating includes ablating of at least a portion of said at least one wafer-level redistribution circuit and said outer passivation layer.

8. The method, as recited in claim 5, wherein said isolating includes etching of at least a portion of said at least one wafer-level redistribution circuit and said outer passivation layer.

9. A method for manufacturing wafer-level testable dice, comprising:

forming a plurality of dice on a semiconductor wafer, said plurality of dice each including at least one die contact; and

forming at least one wafer-level redistribution circuit on each of said plurality of dice for interconnection with others of said plurality of dice, said at least one wafer-level redistribution circuit including a redistribution circuit, a bus conductor traversing each of said plurality of dice for electrically coupling with at least another one of said plurality of dice and at least one bus conductor for coupling said redistribution circuit to said bus conductor.

10. The method, as recited in claim 9, further comprising isolating at least one of said at least one die contact on nonfunctional dice of said plurality of dice on said semiconductor wafer.

11. The method, as recited in claim 9, further comprising probing each of said plurality of dice to determine functional and nonfunctional dice of said plurality of dice.

12. A method for fabricating a wafer-level testable semiconductor component, comprising:

forming a plurality of dice on a semiconductor wafer, said plurality of dice each including at least one die contact;

forming at least one wafer-level redistribution circuit on each of said plurality of dice for interconnection with others of said plurality of dice, said at least one wafer-level redistribution circuit including a redistribution circuit, a bus conductor traversing each of said plurality of dice for electrically coupling with at least another one of said plurality of

dice and at least one bus conductor for coupling said redistribution circuit to said bus conductor;

isolating said at least one die contact on each nonfunctional die of said plurality of dice;

testing functional dice of said plurality of dice while integral with said semiconductor wafer; and

singulating one of said functional dice of said plurality of dice from said semiconductor component.

13. The method, as recited in claim 12, wherein said isolating further comprises probing each of said plurality of dice to determine said functional dice and said nonfunctional dice of said plurality of dice.

14. The method, as recited in claim 12, further comprising burning-in said semiconductor component while said semiconductor component is integral with said semiconductor wafer.

15. A method for retrofitting an existing wafer layout for wafer-level testing, comprising:

on a semiconductor wafer including a plurality of dice with each die including at least one die contact, forming at least one wafer-level redistribution circuit on each of said plurality of dice for interconnection with others of said plurality of dice, said at least one wafer-level redistribution circuit including a redistribution circuit for coupling said at least one die contact to a respective bumped contact, a bus conductor traversing at least a portion of each of said plurality of dice for electrically coupling with at least another one of said plurality of dice, said at least one bus conductor for coupling said redistribution circuit to said bus conductor; and

isolating at least one die contact on each nonfunctional die of said plurality of dice.

16. The method, as recited in claim 15, wherein said forming further comprises forming an outer passivation layer over said redistribution circuit and said bus conductor.

17. The method, as recited in claim 15, wherein said isolating further comprises probing each of said plurality of dice to determine functional dice and said nonfunctional dice of said plurality of dice.

18. The method, as recited in claim 16, wherein said isolating includes removing a portion of said outer passivation layer over said at least one of said wafer-level redistribution circuit and forming an open circuit between said at least one die contact and said bus conductor on said nonfunctional dice.

19. The method, as recited in claim 18, wherein said isolating includes ablating of at least a portion of said at least one wafer-level redistribution circuit and said outer passivation layer.

20. The method, as recited in claim 18, wherein said isolating includes etching of at least a portion of said at least one wafer-level redistribution circuit and said outer passivation layer.

21. A method for isolating nonfunctional dice from a wafer-level testing configuration, comprising:

forming at least one wafer-level redistribution circuit on each of said plurality of dice for interconnection with others of said plurality of dice, said at least one wafer-level redistribution circuit including a redistribution circuit for coupling at least one die contact to a respective bumped contact, a bus conductor traversing each of said plurality of dice for electrically coupling with at least another one of said plurality of dice and at least one bus conductor for coupling said redistribution circuit to said bus conductor; and

isolating at least one die contact on each nonfunctional die of said plurality of dice.

22. The method, as recited in claim 21, further comprising forming an outer passivation layer over said at least one redistribution circuit and said at least one bus conductor.

23. The method, as recited in claim 22, wherein said outer passivation layer is selectively removable over at least a portion of one of said at least one redistribution circuit and at least one conductor for forming an electrical open circuit between said at least one die contact and said at least one bus conductor when a die of said plurality of dice is determined to be defective.

24. The method, as recited in claim 23, wherein said isolating includes etching said at least one redistribution circuit to form said electrical open circuit.

25. The method, as recited in claim 23, wherein said isolating includes ablating said at least one redistribution circuit by a laser to form said electrical open circuit.